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PTO/SB/08a (08-03)

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	10/749,080
				Filing Date	December 30, 2003
				First Named Inventor	Cheng et al.
				Art Unit	TBD 2818
				Examiner Name	TBD LONG TRAN
Sheet	1	of	2	Attorney Docket Number	TSM03-0549

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
UKT		US- 6,538,277 B2	03-25-2003	Sung et al.	
		US- 6,566,706 B1	05-20-2003	Wang et al.	
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet

2

of

2

Attorney Docket Number

Complete if Known

Application Number

10/749,080

Filing Date

December 30, 2003

First Named Inventor

Cheng et al.

Art Unit

TBD 2818

Examiner Name

TBD LONG TRAN

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
UET		ERTL, FRANK et al., "Vertical transistors with ultra-short channel lengths," <i>Fundamental research in semiconductor electronics - Annual Report 2000</i> , (2000) pp. 90-91.	
UET		GÖHLER, LUTZ. et al., "A Compact Model for Depletion MOSFETs in Smart Power Applications Including Source and Drain Resistance," (Date Unknown) 5 pages.	
UET		MANNERS, DAVID, "Infineon Looks to NROM," <i>Electronics Weekly</i> , (May 28, 2001) http://www.reed-electronics.com/electronicnews .	
UET		SHEPARD, KENNETH, et al., "Static Noise Analysis for Digital Integrated Circuits in Partially-Depleted Silicon-On-Insulator Technology," <i>Proceedings of the Design Automation Conference</i> , Los Angeles, California, (June 2000) 4 pages.	
UET		STOCKINGER, MICHAEL, "2.3 Drain-Induced Barrier Lowering," (January 05, 2000) http://www.iue.tuwien.ac.at/phd/stockinger/node15.html .	

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